Optimal IC Technologies, Inc.

Optimal IC Technologies is in the business of helping semiconductor companies maximize yields of their chips and be more profitable. For many of those companies, this means improving shareholder value. Optimal IC Technologies is in business to help semiconductor manufacturers optimize integrated circuit (IC) power, performance, utilization and yield across the full spectrum of ICs ("chips") designed and manufactured by companies in the global semiconductor industry. We are a business where people want to work that encourages and fosters both personal and professional growth in a mutually beneficial professional environment. The company is capitalizing on tremendous opportunities to provide high-value products that would maximize financial returns or rewards to investors, executives, employees and founders. This company was founded in early 2018 via a relationship with a research physicist at the University of Southern California who sought to commercialize the patented technologies he and a team of graduate students developed at USC. The physicist suggested that Optimal IC Technologies work with the Steven's Institute at USC to license the technology. The company's legal address is 7021 Ranger Dr, Fort Collins, CO 80526. The company is owned by Lewis Hartle. Technical consultants include Dr. Young Cho, Ph.D., University of Southern California, and Andrew Goodney, Ph.D., University of Southern California.

Optimal IC Technologies Inc. objectives:

1. Develop professional business plan by October 1, 2018
2. Secure licensing agreement with USC and enter into development agreement by December 31, 2018
3. Develop professional presentation to pitch and secure $1,500,000 in funding by March 31, 2021
4. Use USC to begin product development, prototype, and demonstration. Find Engineering firm to support development through testing and complete commercialization by June 30 2021.
5. Identify potential business partners in Q1 2021, secure partnership by June 30, 2021.
6. Prove concept and develop revenue stream (license agreement) or sell Optimal IC Technologies December 31, 2021.

Optimal IC Technologies is a Corporation registered in the State of Colorado, U.S.A. Optimal IC Technologies will issue stock to the following parties:

- Lewis Hartle 40%
- Investor 30%
- David Webb 10%
- USC Stevens Center for Innovation 5%
- Young Cho 5%
- Andrew Goodney 5%
- Charles Webb 5%

Optimal IC Technologies develops and markets the following products for testing and simulating integrated circuits (ICs) across the spectrum of design, verification, validation, manufacturing, and testing processes. These products map the power consumption and temperature dissipation of ICs at the subcomponent level (extremely small circuit geometries, e.g., < 0.5 micron).

Product 1: IC production yield improvement

Areas of a given chip ("subcomponents") can have poor heat dissipation due to variables in the manufacturing process that produce minor differences in chips with the exact same design. Poor heat dissipation in any one area (a "hot spot") can lead to excessive thermal overload in that area, which in turn destroys the entire chip. This Optimal IC Technologies product identifies such hot spots, and reduces clock speeds within the circuitry of those hot spots to mitigate destructive potential. This results in reduced chip failures and improved yields at the end of the packaging stage of the manufacturing process.

Product 2: IC performance optimization

This Optimal IC Technologies product enables all IC subcomponents that are not prone to thermal overloads to be tuned for maximum clock speeds within the designed tolerances of a chip's circuitry. This, in turn, maximizes performance of the chip.

Product 3: IC power optimization

This Optimal IC Technologies product identifies circuits and subcomponentry with good heat dissipation, and tunes them with reduced clock speeds. This enables the chip to meet designed performance specifications with reduced power consumption (i.e., optimal power efficiency).

Product 4: IC security integrity

This Optimal IC Technologies product scans an integrated circuit on a chip-by-chip basis to identify hardware and software vulnerabilities (e.g., back doors that may be exploited as ways to evade security of host systems). Because the power measurements for each chip are extremely accurate and high resolution, these measurements are used to "fingerprint" each IC for every chip-software combination. Since each chip-software combination has a unique power/temperature fingerprint, the extracted fingerprint can be compared to original design specifications. This enables identification of maliciously modified chips, and/or the presence of any malware or erroneous software on a particular chip. This not only improves security of chips, but security of systems by reducing or eliminating the potential for hacks or malicious insertion or exploitation of hidden back-door vulnerabilities.

Product 5: IC power and performance simulation

This product is a pre-fabrication simulation software. The best power simulation software in the industry today gives results that are unreliable (about +/-30 percent off from HSPICE simulators), mainly because currently available power simulation software is 100,000-1,000,000 times slower than HSPICE. Optimal IC Technologies' software employs similar underlying technology as HSPICE, but is about 1,000-10,000 faster than HSPICE and

provides the same level of accuracy as HSPICE. This power simulation software enables designers/ manufacturers to do what they've not been able to do effectively: modify chip designs in preproduction to maximize IC performance and/or efficiency of energy required of the chip.

The global market for semiconductors includes everything from the microprocessors used in PCs to the memory chips used in thumb drives to the complex logic chips that harness processing power for computers, networks and all kinds of other IT applications. The Semiconductor Industry Association's 2020 State of the Industry report estimates the global semiconductor sales will reach $426 billion this year, and rise six percent to $452 billion in 2021.

The semiconductor (IC) market is segmented into four general types: memory chips, processor chips, logic chips and analog devices. Memory chips include dynamic random-access chips, or DRAM; static random-access chips, or SRAM, and flash memory. Processors include GPUs (graphics processing units such as an AMD Radeon), MPUs (microprocessors such as Intel's Core chips), and a wide array of embedded MCUs (microcontrollers) used in everyday appliances, autos, machinery and so on. Logic chips include the support chips that surround a microprocessor (chipsets) typically found on a motherboard, although much of this logic is increasingly integrated into SoCs (system-on-a-chip ICs) and GPUs/MPUs themselves as on-chip circuit geometries approach 10nm in size. Finally, analog chips, which include DSPs (digital signal processors), are primarily used in low-cost/high-volume markets.

Semiconductor manufacturing typically involves the production of chips cut from wafers of a prefabricated, specialized silicon. Since the industry's earliest days, the process of mass production of ICs center on a standardized size (diameter) of the wafer IC the dies are cut from. Most chips today are manufactured with equipment geared to handle 200mm diameter wafers, but there is a steady trend with fabs and foundries toward adoption of a 300 mm wafer diameter as the standard for the next decade or more. The larger the wafer, the more chips it can produce (similar to a farmer's plot of arable land). Moore's Law continues to apply as IC circuit geometries shrink from 1.0 micron sizes in the 1990s to nodes approaching 10 nanometers (an atom of hydrogen is approximately 0.10nm by comparison): IC manufacturers are doubling the number of transistors packed into the same area of silicon every two years.

The chip manufacturing process involves several phases. First, a chip is designed using electronic design automation (EDA) software, which is also referred to as electronic computer-aided design (ECAD). These are software tools for designing electronic systems such as integrated circuits and printed circuit boards. The tools work together in a design flow that IC designers use to design and analyze functionality of entire semiconductor chips. Since a modern IC can have billions of components, EDA tools are essential for their design. Once the design is virtually tested and complete, designers use synthesis software tools to "translate" the design into manufacturable hardware, or in the case of ICs, a "real" chip.

Manufacturing itself begins with creation of the IC substrate, which is almost always silicon (specifically, the chemically engineered silicon ingots from which wafers are sliced). The front-end manufacturing process involves slicing the ingots into wafers, which are then sanded and polished to incredibly smooth surface tolerances. Wafers are then subjected to a series of chemical etching and thin-film application processes to "lay down" the circuitry as described by the EDA synthesis software for a given design. The process is akin to how photographs are developed (the "photolithography" process) in which a reactive layer (thin film) of photosensitive chemical reacts to light it is briefly exposed to, then "develops." The wafer is then "washed" to shed the remaining film that did not react, leaving an etch or conductive material behind. Layer after layer in this

process creates the circuitry on each of the dies on a wafer, which can "hold" anywhere from a few dies to hundreds within the wafer's diameter depending upon the size of the wafer and the chip design. Once the lithographic processes are complete, and the ICs are "built," they are cut out of the wafer into uniform dies. In die form, the chips are tested for yield, then moved to the packaging process. Packaging typically involves bonding the die to the inside of an insular plastic enclosure with conductive connections to the exterior of the package (the connections made to a printed circuit board, for example). Once the dies are bonded into the plastic packages, they are tested again for quality control before finally entering the product (cardboard) packaging and stocked or shipped to customers.

This last stage, or back-end of chip manufacturing is the packaging process. This is the stage is where a number of factors create opportunity for Optimal IC Technologies.

First, chips that are tested for QC in a packaged state are subjected to "one-size-fits-all" types of testing that can overwhelm one or more of the hundreds of components or cores that comprise a chip. Such tests can literally ruin an entire IC by pushing too much voltage through subcomponent core circuits that then cause the circuits to overheat and burn up. These are common tests performed at foundries (e.g. TSMC, or UMC) and semiconductor companies with their own fabs (e.g., Intel, or Micron). Not all chips with the same design are prone to this problem, but those with otherwise acceptable variances in substrate composition or even packaging can be subject to excessive thermal dissipation that destroys the circuit, which effectively ruins the chip. This problem has implications for production yields, which in the semiconductor industry translate directly to profits (more "good chips" in a batch produced from relative fixed cost of manufacturing results in greater profit).

Second, semiconductor foundries and fabs do not have the means to determine the test thresholds (the point a given test can cause a chip to fail due to the test itself) of each and every chip's subcomponents and cores. They must determine a safe threshold they can rely upon for current capacity to ensure the highest yields out of post-production testing, or within a chip's application environment. This "blind" approach is not conducive to a.) maximization of the performance potential of a given chip, or b.) optimization of power consumption of a given chip in its packaged state. In other words, most ICs, particularly high-performance graphics and central processor chips, aren't realizing the true potential of their processing power or their ability to perform at optimal energy consumption. Optimal IC Technologies' IP provides the means to map each and every chip in a way that easily identifies common variations in the manufacturing process. Such variations can cause subcomponents and cores within a chip to possess different thresholds of current capacity. Our technology makes it possible to tune each packaged chip within seconds (in some cases, milliseconds) to ensure the design potential of the chip is maximized - either for low-power consumption or for the highest performance attainable.

Third, there is a major and ever-increasing opportunity to address security concerns with hardware, especially in mass-market devices such as mobile phones and portable PCs. Optimal IC's technology's enablement of visibility into power and performance of all areas of each and every chip's circuitry (again, as each chip is coming off the production line in a final packaged state) also has implications for improved security at the IC level. A chip designer, for example, can confirm whether a foundry or fab has changed a design in any way by virtue of comparing random volume-produced packaged chips with pre-production "control" chips that were mapped by the technology. A semiconductor company can then confirm if circuitry had been changed or added by a foundry, which in some cases can be deliberately done to create hidden back-door security breaches in chips used in widespread applications, such as a processor in a mobile phone or a laptop PC.

Fourth, chip yields are compromised at the point of testing packaged chips. Yields of semiconductors are directly related to profit; the higher the yields, profits are commensurately higher. A "dirty secret" in the IC industry is that yields at the post-packaging point the manufacturing process are not equal to the yields of ICs cut from wafers. Wafer-cut die yields greater than 80 percent are accepted as good, but can dip below 50 percent during the packaging process. The reason is that as circuit geometries, or nodes, continue to get smaller (approaching 10 nanometers today), variations in substrates from die to die (or chip to chip) can cause heretofore unpredictable variations of current carrying capacities at the subcomponent or core levels of a chip's circuitry. A tiny core within a chip of a given design, for example, might burn up (consequently ruining the entire chip) due to a voltage applied during a common quality control check at the end of the manufacturing process. The same core within another chip of the same design, will weather the test voltage without a problem. Without visibility into each and every chip's tolerances down to the granularity of the tiniest cores, chips are prone to failures during this test, which again reduces yield (and profit). Optimal IC's ability to determine tolerances of each and every chip's vast array of circuitry enables fine-tuning of test voltages to ensure a chip does not inadvertently burn up due to common quality testing procedures.

The benefits of Optimal IC's technology are realized primarily by semiconductor manufacturers (both with and without fabs). They can realize maximum yields while gaining critical specification data about each and every chip, specifications that system OEMs value as a means of maximizing the value of their products to end-users.

SWOT Analysis

Optimal IC Technologies is in a unique position to bring products of tremendous value to companies throughout the $475B semiconductor industry. There is no direct competition for any one product, and the spectrum of products addresses different problems that translate directly to bottom-line performance of many IC manufacturers and foundries. Optimal IC also enables IC vendors to offer greater value to their respective customers with performance and power optimization, security and reliability.

Strengths

Greenfield market for a family of products that has no direct competition.

Secure technology license ensures low competition in application space.

Prestigious source of development (USC)

Potential Technical Advisor is an inventor and patent holder of the technologies applied in each product.

Relatively low overhead business (low-volume hardware involved, primarily software)

Weaknesses

New, untested technologies in real world

Lack of market awareness

Early stage funding needed to go to market

Opportunities

Small number of companies can produce big revenue numbers

Applications span multiple markets

Additional applications for base technologies are waiting in the wings

Threats

Lengthy sales cycles

Funding shortfalls for development

Near-term staffing challenges

Management Team

Lewis Hartle is the Chief Executive Officer

Dave Webb is the Vice President of Marketing and Sales

Dr. Young Cho is a senior technology advisor

Dr. Andrew Goodney is a senior technology advisor

https://patents.google.com/patent/US9618547B2

https://patents.google.com/patent/US10386395B1

https://patents.google.com/patent/US10386395B1

Financial Plan	2020	2021	2022	2023	2024	2025
Minimum Annual Royalty March 1, 2020	**$ 10,000**					
Minimum Annual Royalty March 1, 2021		**$ 10,000**				
Minimum Annual Royalty March 1, 2022			**$ -**			
Milestone - establish partnership	**$ 5,000**					
Milestone - first commercial sale	**$ 5,000**					
Patent expense July 1, 2019	**$ 20,000**					
Patent expense October 1, 2019	**$ 20,000**					
Patent expense February 14, 2020	**$ 20,000**					
CEO	**$ 43,750**	**$ 175,000**	**$ 175,000**	**$ 175,000**	**$ 175,000**	**$ 175,000**
VP Marketing and Sales	**$ 31,250**	**$ 125,000**	**$ 125,000**	**$ 125,000**	**$ 125,000**	**$ 125,000**
Product Development	**$ 150,000**	**$ 245,500**		**$ 10,000**	**$ 10,000**	**$ 10,000**
Marketing	**$ 25,000**	**$ 50,000**	**$ 25,000**	**$ 25,000**	**$ 25,000**	**$ 25,000**
Sales		**$ 100,000**	**$ 105,000**	**$ 115,500**	**$ 127,050**	**$ 139,755**
Legal, Accounting, Admin	**$ 10,000**	**$ 2,500**	**$ 2,000**	**$ 2,000**	**$ 2,000**	**$ 2,000**
USC royalty 2% of sales	**$ -**	**$ -**	**$ 20,000**	**$ 50,000**	**$ 100,000**	**$ 150,000**
	$ 340,000	**$ 708,000**	**$ 452,000**	**$ 502,500**	**$ 564,050**	**$ 626,755**
Revenue		**$ 250,000**	**$ 1,000,000**	**$ 2,500,000**	**$ 5,000,000**	**$ 7,500,000**
Profit	**$ (340,000)**	**$ (458,000)**	**$ 548,000**	**$ 1,997,500**	**$ 4,435,950**	**$ 6,873,245**
		$ (798,000)	$ (250,000)	$ 1,747,500	$ 6,183,450	$ 13,056,695